REMARKS

Claims 1-7, 9-23, and 27-34 are pending.

Claims 1, 3, 10, 18, and 27 have been amended to correct typographical informalities. Support for these changes is believed to be self-evident from the claims. No new matter has been added.

§102 Rejections

In the action mailed February 28, 2005, claims 18 and 27 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent Publication No. 2003/0115424 to Bachand et al. (hereinafter "Bachand").

Claim 18 relates to a method that includes performing a trace operation and performing a compression operation. Claim 27 relates to an apparatus for use in a trace buffer. The apparatus includes instructions residing on a machine-readable medium. The instructions cause the machine to perform a trace operation and perform a compression operation.

The rejections contend that Bachand's snoop blocking is somehow related to the performance of a trace operation and the performance a compression operation. Applicant respectfully disagrees.

Bachand is directed toward maintaining cache coherency in a multi-agent architecture. *See* Bachand, para. [0002]. In a

multi-agent architecture, two or more agents may require data from the same memory location at the same time. *See* Bachand, para. [0003]. Cache coherency is maintained when such agents use the most current copy of the data. *Id.*

A snoop response is a message between agents on a bus that allows a requesting agent to identify if other agents currently possess copies of data. *See* Bachand, para. [0009]. In traditional systems, when the requesting agent requires data that is held in a modified state by another agent, the other agent can provide the modified data to the requesting agent. *Id.* Generally, data is provided to the requesting agent from an external memory. *Id.*

In Bachand's system, however, a snoop queue 250 receives data requests for new transactions before a snoop probe is released. *See* Bachand, para. [0033]. If a cache coherency check is required, Bachand's snoop queue provides an address of the newly requested data to an external transaction queue and awaits a return signal that indicates whether the address of the newly requested data matches the address of a pending, posted transaction data. *Id.* The external transaction queue compares the address of the newly requested data with addresses of pending posted transaction data using match detection logic 244 to generate the return signal. *See* Bachand, para. [0036-0037].

If the comparison shows that the address of the newly requested data is the same as an address of a pending transaction data, then Bachand blocks the snoop probe (by enabling a blocking bit) and waits for such pending transaction data to be globally observed. *See* Bachand, para. [0033-0034].

It is respectfully submitted that Bachand has nothing to do with either the performance of a trace operation or the performance of a compression operation, as claimed.

In regard to the performance of a trace operation, the trace operations in claims 18 and 27 include the storage of fetched instructions in a trace buffer. In contrast, Bachand's entire system is dedicated to determining when and how data is to be accessed. Neither Bachand's newly requested data nor Bachand's pending transaction data have been accessed when they are compared. Indeed, if Bachand's snoop queue or Bachand's were to store fetched instructions, Bachand's system could come to a standstill. A snoop probe could be halted indefinitely since there would be no subsequent change to the already-fetched instructions.

Further, the storage of fetched instructions includes the storage of an address pair corresponding to a loop. Neither Bachand's snoop queue nor Bachand's external transaction queue describe or suggest the storage of address pairs corresponding

to loops. Rather, they appear to store solitary addresses of transaction data.

In regard to the performance of a compression operation, the rejection contends that Bachand's comparison of addresses of pending transaction data with the addresses of the newly requested data and halting of a snoop probe (by setting a blocking bit) somehow results in a compression. Applicant respectfully disagrees.

Bachand's comparison of addresses and halting of a snoop probe does not compress anything. The halting of a snoop probe results in the snoop probe being unreleased. Therefore Bachand can fairly be said to maintain or even expand the size of snoop queue 250. No compression is achieved.

Accordingly, claims 18 and 27, and the claims dependent therefrom, are not anticipated by Bachand.

§103(a) Rejections

Claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 3,975,717 to Panigrahi (hereinafter "Panigrahi") and Bachand.

Claim 1 relates to a trace buffer circuit. The circuit includes a first comparator and a second comparator. The first comparator is to compare a new branch target address corresponding to a loop in a first holding register to a stored

branch target address in a first end register. The second comparator is to compare a new branch source address corresponding to the loop in a second holding register to a stored branch source address in a first adjacent register.

The rejection of claim 1 contends that Bachand's observation detection logic is both the first comparator and the second comparator.

Applicant respectfully disagrees. Even if one set of logic could somehow form two different comparators performing two different comparisons (which applicant does not concede), Bachand's observation detection logic fails to describe or suggest the claimed comparators. As discussed above, Bachand compares the address of newly requested data with addresses from pending posted transaction data. *See* Bachand, para. [0036-0037]. These compared addresses are neither branch target addresses nor branch source addresses. Rather, they are simply generic data addresses.

Panigrahi does nothing to remedy these deficiencies in Bachand. Panigrahi's charge-coupled device register does not include any comparators at all, much less comparators that compare branch target addresses and branch source addresses.

Accordingly, claim 1, and the claims dependent therefrom, are not obvious over Panigrahi and Bachand.

Claim 13 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Panigrahi, Bachand, and U.S. Patent No. 5,553,010 to Tanihara et al. (hereinafter "Tanihara").

Claim 13 relates to a pipelined processor. The processor includes a trace buffer circuit. The trace buffer circuit includes a plurality of interconnected registers. These include a first end register to input and output addresses of fetched instructions during a trace operation.

The rejection contends that Bachand's observation detection logic 246 is a trace buffer circuit.

Applicant respectfully disagrees. As discussed above, Bachand's logic compares the address of newly requested data with addresses of pending posted transaction data. See Bachand, para. [0036-0037]. This comparison does not have anything to do with a trace operation. For example, the comparison does not involved fetched instructions at all. Rather, Bachand maintains cache coherency through a comparison between pending transaction and newly requested data.

Indeed, the comparison of an address of newly requested data with the addresses of already-fetched instructions could bring Bachand's system to a standstill. In particular, a snoop probe could be halted indefinitely since there would be no subsequent change to the already-fetched instructions.

Panigrahi and Tanihara do nothing to remedy these deficiencies in Bachand. Panigrahi's charge-coupled device register does not involve trace buffer circuits at all, much less a trace buffer circuit that includes a first end register to input and output addresses of fetched instructions during a trace operation. Tanihara describes a data shifting circuit of a central processor and has nothing to do with either trace buffer circuits or trace operations.

Accordingly, claim 13, and the claims dependent therefrom, are not obvious over Panigrahi, Bachand, and Tanihara.

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: April 28, 2005

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